TABLE 3a. Mnemonics and Layouts of Instructions with Opcodes 00 through 2F.

Opcode	Instruction	Mnemonic	Type	Subop	31 30 29	28 27 26 25 24 23	22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
00	Jump	jmp	0		p p p	0 0 0 0 0 0	i i i i i i i i i i i i i i i i i i i i i i i
01	Jump and Link	jmp.link	0		p p p	0 0 0 0 0 1	i i i i i i i i i i i i i i i i i i i i i i i
02	Jump Register	jmp.reg	1		p p p	0 0 0 0 1 0	r r r r r i i i i i i i i i i i i i i i i i i
03	Jump Register and Link	jmp.reg.link	1		p p p	0 0 0 0 1 1	r r r r r i i i i i i i i i i i i i i i i i i
04	Load Immediate High	loadi.hi	1		p p p	0 0 0 1 0 0	r r r r r i i i i i i i i i i i i i i i i i i
05	Load Immediate Low	loadi.lo	1		p p p	0 0 0 1 0 1	r r r r r i i i i i i i i i i i i i i i i i i
06					p p p	0 0 0 1 1 0	
07	Trap	trap	0		p p p	0 0 0 1 1 1	i i i i i i i i i i i i i i i i i i i i i i i
08	Compare	cmp	5a		p p p	0 0 1 0 0 0	r r r r r r r r r r p p p p p p t t t t
09	Compare Immediate	cmpi	5b		p p p	0 0 1 0 0 1	r r r r r i i i i i i i i p p p p p p t t t t
0A	Test Bit	testbit	5b		p p p	0 0 1 0 1 0	r r r r r i i i i i i i i p p p p p p t t t t
0B	Change Predicate Set	changepr	5b		p p p	0 0 1 0 1 1	r r r r r i i i i i i i i p p p p p p t t t t
0C	Change Predicate Set and Load	changepr.ld	5b		p p p	0 0 1 1 0 0	r r r r r i i i i i i i i p p p p p p t t t t
0D					p p p	0 0 1 1 0 1	
0E					p p p	0 0 1 1 1 0	
0F					p p p	0 0 1 1 1 1	

TABLE 3b. Mnemonics and Layouts of Instructions with Opcodes 00 through 2F.

Opcode	Instruction	Mnemonic	Type	Subop	31 30 29	28 27 26 25 24 23	22 21 20 19 18	17 16 15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
10	Load 1 Byte	load.1	2		p p p	0 1 0 0 0 0	r r r r r	r r r r r	i i i i i i i i i i i i i
11	Load 2 Byte	load.2	2		p p p	0 1 0 0 0 1	r r r r r	r r r r r	i i i i i i i i i i i i i
12	Load 4 Byte	load.4	2		p p p	0 1 0 0 1 0	r r r r r	r r r r r	i i i i i i i i i i i i i
13	Load 8 Byte	load.8	2		p p p	0 1 0 0 1 1	r r r r r	r r r r r	i i i i i i i i i i i i i
14	Load 1 Byte Update	load.1.update	2		p p p	0 1 0 1 0 0	r r r r r	r r r r r	i i i i i i i i i i i i i
15	Load 2 Byte Update	load.2.update	2		p p p	0 1 0 1 0 1	r r r r r	r r r r r	i i i i i i i i i i i i i
16	Load 4 Byte Update	load.4.update	2		p p p	0 1 0 1 1 0	r r r r r	r r r r r	i i i i i i i i i i i i i
17	Load 8 Byte Update	load.8.update	2		p p p	0 1 0 1 1 1	r r r r r	r r r r r	i i i i i i i i i i i i i
18	Store 1 Byte	store.1	2		p p p	0 1 1 0 0 0	r r r r r	r r r r r	i i i i i i i i i i i i i
19	Store 2 Byte	store.2	2		p p p	0 1 1 0 0 1	r r r r r	r r r r r	i i i i i i i i i i i i i
1A	Store 4 Byte	store.4	2		p p p	0 1 1 0 1 0	r r r r r	r r r r r	i i i i i i i i i i i i i
1B	Store 8 Byte	store.8	2		p p p	0 1 1 0 1 1	r r r r r	r r r r r	i i i i i i i i i i i i i
1C	Store 1 Update	store.1.update	2		p p p	0 1 1 1 0 0	r r r r r	r r r r r	i i i i i i i i i i i i i
1D	Store 2 Update	store.2.update	2		p p p	0 1 1 1 0 1	r r r r r	r r r r r	i i i i i i i i i i i i i
1E	Store 4 Update	store.4.update	2		p p p	0 1 1 1 1 0	r r r r r	r r r r r	i i i i i i i i i i i i i
1F	Store 8 Update	store.4.update	2		p p p	0 1 1 1 1 1	r r r r r	r r r r r	i i i i i i i i i i i i i

TABLE 3c. Mnemonics and Layouts of Instructions with Opcodes 00 through 2F.

Opcode	Instruction	Mnemonic	Type	Subop w/o ss	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
20	Add Immediate	addi	2		p	p	p	1	0	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	i	i	i	i	i	i	i	i	i	i	i	i
21	Subtract Immediate	subi	2		p	p	p	1	0	0	0	0	1	r	r	r	r	r	r	r	r	r	r	r	i	i	i	i	i	i	i	i	i	i	i	i
22	And Immediate	andi	2		p	p	p	1	0	0	0	1	0	r	r	r	r	r	r	r	r	r	r	r	i	i	i	i	i	i	i	i	i	i	i	i
23	Or Immediate	ori	2		p	p	p	1	0	0	0	1	1	r	r	r	r	r	r	r	r	r	r	r	i	i	i	i	i	i	i	i	i	i	i	i
24	Xor Immediate	xori	2		p	p	p	1	0	0	1	0	0	r	r	r	r	r	r	r	r	r	r	r	i	i	i	i	i	i	i	i	i	i	i	i
25	Shift Left Logical Immediate	slli	2		p	p	p	1	0	0	1	0	1	r	r	r	r	r	r	r	r	r	r	r	i	i	i	i	i	i	i	i	i	i	i	i
26	Shift Right Arithmetic Immediate	srai	2		p	p	p	1	0	0	1	1	0	r	r	r	r	r	r	r	r	r	r	r	i	i	i	i	i	i	i	i	i	i	i	i
27	Shift Right Logical Immediate	srli	2		p	p	p	1	0	0	1	1	1	r	r	r	r	r	r	r	r	r	r	r	i	i	i	i	i	i	i	i	i	i	i	i
28	Deposit	deposit	3		p	p	p	1	0	1	0	0	0	r	r	r	r	r	r	r	r	r	r	r	p	p	p	p	p	p	p	L	L	L	L	L	L
29	Extract	extract	3		p	p	p	1	0	1	0	0	1	r	r	r	r	r	r	r	r	r	r	r	p	p	p	p	p	p	p	L	L	L	L	L	L
2A	Shift Right Pair	shrp	4c		p	p	p	1	0	1	0	1	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	i	i	i	i	i	i	i
2B					p	p	p	1	0	1	0	1	1																									
2C					p	p	p	1	0	1	1	0	0																									
2D					p	p	p	1	0	1	1	0	1																									
2E					p	p	p	1	0	1	1	1	0																									
2F					p	p	p	1	0	1	1	1	1																									

TABLE 4a. Subop Definitions for Packed ALU Instructions (opcode = 30).

Opcode	Instruction	Mnemonic	Type	*Subop w/o sw	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
30	Packed Add 1 Byte	padd.1	4a	0	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	0	0	0	0
30	Packed Add 2 Byte	padd.2	4a	0	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	0	0	0	1
30	Packed Add 4 Byte	padd.4	4a	0	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	0	0	1	0
30	Packed Add 8 Byte	padd.8	4a	0	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	0	0	1	1
30	Packed Add 1 Byte Unsigned Saturation	padd.1.u	4a	1	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	0	1	0	0
30	Packed Add 2 Byte Unsigned Saturation	padd.2.u	4a	1	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	0	1	0	1
30	Packed Add 4 Byte Unsigned Saturation	padd.4.u	4a	1	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	0	1	1	0
30	Packed Add 8 Byte Unsigned Saturation	padd.8.u	4a	1	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	0	1	1	1
30	Packed Add 1 Byte Signed Saturation	padd.1.s	4a	2	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	1	0	0	0
30	Packed Add 2 Byte Signed Saturation	padd.2.s	4a	2	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	1	0	0	1
30	Packed Add 4 Byte Signed Saturation	padd.4.s	4a	2	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	1	0	1	0
30	Packed Add 8 Byte Signed Saturation	padd.8.s	4a	2	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	1	0	1	1
30	Packed Add Increment 1 Byte	paddincr.1	4a	3	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	1	1	0	0
30	Packed Add Increment 2 Byte	paddincr.2	4a	3	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	1	1	0	1
30	Packed Add Increment 4 Byte	paddincr.4	4a	3	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	1	1	1	0
30	Packed Add Increment 8 Byte	paddincr.8	4a	3	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	0	0	1	1	1	1

Remarks

* The subop w/o sw field excludes the two lowest-order bits (bits 0 and 1 of the instruction) of the subop. These two bits are used to indicate the subword size of the instruction.

TABLE 4b. Subop Definitions for Packed ALU Instructions (opcode = 30).

Opcode	Instruction	Mnemonic	Type	*Subop w/o sw	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
30	Packed Subtract 1 Byte	psub.1	4a	4	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 0 0 0 0
30	Packed Subtract 2 Byte	psub.2	4a	4	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 0 0 0 1
30	Packed Subtract 4 Byte	psub.4	4a	4	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 0 0 1 0
30	Packed Subtract 8 Byte	psub.8	4a	4	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 0 0 1 1
30	Packed Subtract 1 Byte Unsigned Saturation	psub.1.u	4a	5	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 0 1 0 0
30	Packed Subtract 2 Byte Unsigned Saturation	psub.2.u	4a	5	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 0 1 0 1
30	Packed Subtract 4 Byte Unsigned Saturation	psub.4.u	4a	5	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 0 1 1 0
30	Packed Subtract 8 Byte Unsigned Saturation	psub.8.u	4a	5	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 0 1 1 1
30	Packed Subtract 1 Byte Signed Saturation	psub.1.s	4a	6	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 1 0 0 0
30	Packed Subtract 2 Byte Signed Saturation	psub.2.s	4a	6	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 1 0 0 1
30	Packed Subtract 4 Byte Signed Saturation	psub.4.s	4a	6	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 1 0 1 0
30	Packed Subtract 8 Byte Signed Saturation	psub.8.s	4a	6	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 1 0 1 1
30	Packed Subtract Decrement 1 Byte	psubdecr.1	4a	7	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 1 1 0 0
30	Packed Subtract Decrement 2 Byte	psubdecr.2	4a	7	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 1 1 0 1
30	Packed Subtract Decrement 4 Byte	psubdecr.4	4a	7	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 1 1 1 0
30	Packed Subtract Decrement 8 Byte	psubdecr.8	4a	7	p p p 1 1 0 0 0 0 r r r r r r r r r r r r r r r r r r r r r r 0 0 0 1 1 1 1 1

Remarks

* The subop w/o sw field excludes the two lowest-order bits (bits 0 and 1 of the instruction) of the subop. These two bits are used to indicate the subword size of the instruction.

TABLE 4c. Subop Definitions for Packed ALU Instructions (opcode = 30).

Opcode	Instruction	Mnemonic	Type	*Subop w/o sw	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
30	Packed Average 1 Byte	pavg.1	4a	8	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	1	0	0	0	0	0
30	Packed Average 2 Byte	pavg.2	4a	8	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	1	0	0	0	0	1
30	Packed Average 1 Byte Round Away from Zero	pavg.1.raz	4a	9	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	1	0	0	1	0	0
30	Packed Average 2 Byte Round Away from Zero	pavg.2.raz	4a	9	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	1	0	0	1	0	1
30	Packed Subtract Average 1 Byte	psubavg.1	4a	A	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	1	0	1	0	0	0
30	Packed Subtract Average 2 Byte	psubavg.2	4a	A	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	0	1	0	1	0	0	1
30	Packed Shift and Add 1 Bit Left	pshiftadd.1.l	4a	11	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	1	0	0	0	1	0	1
30	Packed Shift and Add 2 Bit Left	pshiftadd.2.l	4a	12	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	1	0	0	1	0	0	1
30	Packed Shift and Add 3 Bit Left	pshiftadd.3.l	4a	13	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	1	0	0	1	1	0	1
30	Packed Shift and Add 1 Bit Right	pshiftadd.1.r	4a	15	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	1	0	1	0	1	0	1
30	Packed Shift and Add 2 Bit Right	pshiftadd.2.r	4a	16	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	1	0	1	1	0	0	1
30	Packed Shift and Add 3 Bit Right	pshiftadd.3.r	4a	17	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	0	1	0	1	1	1	0	1
30	Packed Compare 1 Byte Equal To	pcmp.1.eq	4a	20	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	0	0	0	0	0	0
30	Packed Compare 2 Byte Equal To	pcmp.2.eq	4a	21	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	0	0	0	1	0	1
30	Packed Compare 4 Byte Equal To	pcmp.4.eq	4a	22	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	0	0	1	0	1	0
30	Packed Compare 8 Byte Equal To	pcmp.8.eq	4a	23	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	0	0	1	1	1	1
30	Packed Compare 1 Byte Greater Than	pcmp.1.gt	4a	24	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	0	1	0	0	0	0
30	Packed Compare 2 Byte Greater Than	pcmp.2.gt	4a	25	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	0	1	0	1	0	1
30	Packed Compare 4 Byte Greater Than	pcmp.4.gt	4a	26	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	0	1	1	0	1	0
30	Packed Compare 8 Byte Greater Than	pcmp.8.gt	4a	27	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	0	1	1	1	1	1
30	Packed Maximum 1 Byte	pmax.1	4a	28	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	1	0	0	0	0	0
30	Packed Maximum 2 Byte	pmax.2	4a	29	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	1	0	0	1	0	1
30	Packed Minimum 1 Byte	pmin.1	4a	2A	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	1	0	1	0	0	0
30	Packed Minimum 2 Byte	pmin.2	4a	2B	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	0	1	0	1	1	0	1
30	And	and	4a	30	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	1	0	0	0	0	0	0
30	And Complement	andcm	4a	31	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	1	0	0	0	1	0	0
30	Or	or	4a	32	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	1	0	0	1	0	0	0
30	Xor	xor	4a	33	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	1	0	0	1	1	0	0
30	Not	not	4a	34	p	p	p	1	1	0	0	0	0	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	1	1	0	1	0	0	0	0

Remarks

* The subop w/o sw field excludes the two lowest-order bits (bits 0 and 1 of the instruction) of the subop. These two bits are used to indicate the subword size of the instruction.

TABLE 5. Subop Definitions for Packed Multiply Instructions (opcode = 31).

Opcode	Instruction	Mnemonic	Type	*Subop w/o ss	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
31	Packed Multiply Odd	pmul.odd	4a	0	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 0 0 0 0 0 1
31	Packed Multiply Even	pmul.even	4a	1	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 0 0 0 1 0 1
31	Packed Multiply and Shift Right 0 Bit Arithmetic	pmulshr.0.a	4a	4	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 0 1 0 0 0 1
31	Packed Multiply and Shift Right 8 Bit Arithmetic	pmulshr.8.a	4a	5	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 0 1 0 1 0 1
31	Packed Multiply and Shift Right 15 Bit Arithmetic	pmulshr.15.a	4a	6	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 0 1 1 0 0 1
31	Packed Multiply and Shift Right 16 Bit Arithmetic	pmulshr.16.a	4a	7	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 0 1 1 1 0 1
31	Packed Multiply and Shift Right 0 Bit Logical	pmulshr.0	4a	8	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 1 0 0 0 0 1
31	Packed Multiply and Shift Right 8 Bit Logical	pmulshr.8	4a	9	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 1 0 0 1 0 1
31	Packed Multiply and Shift Right 15 Bit Logical	pmulshr.15	4a	A	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 1 0 1 0 0 1
31	Packed Multiply and Shift Right 16 Bit Logical	pmulshr.16	4a	B	p p p 1 1 0 0 0 1 r r r r r r r r r r r r r r r r 0 0 1 0 1 1 0 1

Remarks

* The subop w/o sw field excludes the two lowest-order bits (bits 0 and 1 of the instruction) of the subop. These two bits are used to indicate the subword size of the instruction.

TABLE 6. Subop Definitions for Packed Shift and Subword Permutation Instructions (opcode = 32).

Opcode	Instruction	Mnemonic	Type	*Subop w/o ss	31 30 29	28 27 26 25 24 23	22 21 20 19 18	17 16 15 14 13	12 11 10 9 8	7 6 5 4 3 2	1 0
32	Packed Shift 2 Byte Left	pshift.2.l	4a	0	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 0 0 0 0 0	0 1
32	Packed Shift 4 Byte Left	pshift.4.l	4a	0	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 0 0 0 0 0	1 0
32	Packed Shift 8 Byte Left	pshift.8.l	4a	0	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 0 0 0 0 0	1 1
32	Packed Shift 2 Byte Right Arithmetic	pshift.2.ra	4a	1	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 0 0 0 0 1	0 1
32	Packed Shift 4 Byte Right Arithmetic	pshift.4.ra	4a	1	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 0 0 0 0 1	1 0
32	Packed Shift 8 Byte Right Arithmetic	pshift.8.ra	4a	1	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 0 0 0 0 1	1 1
32	Packed Shift 2 Byte Right Logical	pshift.2.r	4a	2	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 0 0 0 1 0	0 1
32	Packed Shift 4 Byte Right Logical	pshift.4.r	4a	2	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 0 0 0 1 0	1 0
32	Packed Shift 8 Byte Right Logical	pshift.8.r	4a	2	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 0 0 0 1 0	1 1
32	Mix 1 Byte Left	mix.1.l	4a	10	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 1 0 0 0 0	0 0
32	Mix 2 Byte Left	mix.2.l	4a	10	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 1 0 0 0 0	0 1
32	Mix 4 Byte Left	mix.4.l	4a	10	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 1 0 0 0 0	1 0
32	Mix 1 Byte Right	mix.1.r	4a	11	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 1 0 0 0 1	0 0
32	Mix 2 Byte Right	mix.2.r	4a	11	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 1 0 0 0 1	0 1
32	Mix 4 Byte Right	mix.4.r	4a	11	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	0 1 0 0 0 1	1 0
32	Permute	perm	4a	20	p p p	1 1 0 0 1 0	r r r r r	r r r r r	r r r r r	1 0 0 0 0 0	0 1

Remarks

* The subop w/o sw field excludes the two lowest-order bits (bits 0 and 1 of the instruction) of the subop. These two bits are used to indicate the subword size of the instruction.

TABLE 7. Subop Definitions for Packed Shift and Subword Permutation Instructions with Immediates (opcode = 33).

Opcode	Instruction	Mnemonic	Type	*Subop w/o ss	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
33	Packed Shift Immediate 2 Byte Left	pshifti.2.l	4b	0	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 0 0 0 0 0 1
33	Packed Shift Immediate 4 Byte Left	pshifti.4.l	4b	0	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 0 0 0 0 1 0
33	Packed Shift Immediate 8 Byte Left	pshifti.8.l	4b	0	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 0 0 0 0 1 1
33	Packed Shift Immediate 2 Byte Right Arithmetic	pshifti.2.ra	4b	1	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 0 0 0 1 0 1
33	Packed Shift Immediate 4 Byte Right Arithmetic	pshifti.4.ra	4b	1	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 0 0 0 1 1 0
33	Packed Shift Immediate 8 Byte Right Arithmetic	pshifti.8.ra	4b	1	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 0 0 0 1 1 1
33	Packed Shift Immediate 2 Byte Right Logical	pshifti.2.r	4b	2	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 0 0 1 0 0 1
33	Packed Shift Immediate 4 Byte Right Logical	pshifti.4.r	4b	2	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 0 0 1 0 1 0
33	Packed Shift Immediate 8 Byte Right Logical	pshifti.8.r	4b	2	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 0 0 1 0 1 1
33	Mux Reverse	mux.rev	4b	8	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 1 0 0 0 0 0
33	Mux Mix	mux.mix	4b	9	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 1 0 0 1 0 0
33	Mux Shuffle	mux.shuf	4b	A	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 1 0 1 0 0 0
33	Mux Alternate	mux.alt	4b	B	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 1 0 1 1 0 0
33	Mux Broadcast	mux.brcst	4b	C	p p p 1 1 0 0 1 1 r r r r r r r r r r i i i i i 0 0 1 1 0 0 0 0

Remarks

* The subop w/o sw field excludes the two lowest-order bits (bits 0 and 1 of the instruction) of the subop. These two bits are used to indicate the subword size of the instruction.